REMARKS

Claims 1-35 remain in the application for consideration. In view of the following remarks, Applicant respectfully requests reconsideration and allowance of the subject application.

Allowable Subject Matter

Claims 3-11 and 26-34 are objected to by the Office. Applicant thanks the Examiner for the indication of allowable subject matter.

Double Patenting Rejections

Claims (15 & 19) and 16-18 stand rejected under the judicially created doctrine of double patenting as being unpatentable over claims 1, and 2-4 of U.S. Patent No. 6,687,872, respectively. The Applicant respectfully requests that the Office holds the rejections in abeyance until the application is allowed.

Claims (1 & 2) and 12 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 6,687,872. The Applicant respectfully requests that the Office holds the rejections in abeyance until the application is allowed.

Claims 20 and 21-23 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 7 and 8-10 of U.S. Patent No. 6,687,872, respectively. The Applicant respectfully requests that the Office holds the rejections in abeyance until the application is allowed.

Claims (24 & 25) and 35 stand rejected under the judicially created doctrine of obviousness type double patenting as being unpatentable over claims 1 and 3 of U.S. Patent No. 6,687,872. The Applicant respectfully requests that the Office holds the rejections in abeyance until the application is allowed.

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§ 103 Rejections

Claims 13-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 4,996,690 to George et al. (hereinafter "George).

10 Before undertaking a discussion regarding the substance of the Office's rejections, the following discussion of George is included in order to assist the Office in appreciating the patentable distinctions between this reference and the claimed subject matter in this application.

15 **The George Reference**

George describes a communication system that includes a parity digit generator. The described purpose of the parity digit generator is for generating ECC parity digits or check digits. The parity digit generator monitors a high speed data bus and control line between a buffer manager and a tape formatter. 20 Data that passes over the high speed data bus is simultaneously sent to the parity digit generator over a data bus. Parity digits are calculated by the parity digit generator, transferred over a data bus and stored in parity memory for future processing. The parity digit generator also controls the placement of the calculated parity digits within the parity memory. *See George, Col. 5, Lines 56-* 25 *68.*

The Claims

Claim 13 recites a method of calculating parity segments comprising [emphasis added]:

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- providing a parity calculation module configured to calculate one or more parity segments, the parity calculation module being embodied as an application-specific integrated circuit (ASIC);
- with the ASIC:
  - receiving one or more data segments that are to be used to calculate one or more parity segments;
  - ***receiving one or more parity coefficients that are to be used to calculate the one or more parity segments;***
  - operating on the one or more data segments and the one or more parity coefficients to provide an intermediate computation result;
  - writing the intermediate computation result to one or more local buffers on the ASIC;
  - using the intermediate computation result from the one or more local buffers to calculate one or more parity segments; and
  - providing feedback from the one or more local buffers to one or more mathematical operator components that are configured to perform said operating, wherein said feedback on a first pass through the one or more mathematical operator components does not affect computations performed by the one or more mathematical operator components.

In making out a rejection of this claim, the Office fails to argue that George discloses or suggests a method in which one or more parity coefficients are received that are to be used to calculate the one or more parity segments. The Office's failure is understandable as George does not disclose this subject matter. Rather, George describes three methods for calculating parity digits as shown in the following excerpt:

> Calculation of the parity digits can occur by one of three methods. The first method calculates intermediate results of parity digits after each byte of data is transferred to the data sink. The second method calculates one or more intermediate result parity digits after each block of data is transferred to the data sink. The third method encodes parity digits after an entire data interval is transferred to the data sink. The first method calculates parity digits on an ongoing basis whereas, the second and third methods

> calculate parity digits after a particular segment of data is processed; a block of data by the second method and a data interval by the third method. *George, Col. 3, Lines 3 to 15.*

None of the three disclosed methods mention how the parity digits are calculated using a coefficient. Indeed, the only mention of a coefficient in George is included in the following excerpt:

> Parity(PARBLK+j-1, i)=Parity(PARBLK+j, i) XOR g(r-j) *FDBK
> where parity(PARBLK+j-1, i) is the parity memory location of the i.sup.th parity digit in the j-1th parity block, parity(PARBLK+j, i) is equal to the i.sup.th parity digit associated with the i.sup.th data byte in the +j.sup.th parity digit block; g(r-j) is equal to the coefficient of the r-j.sup.th element of the generator polynomial, and, FDBK is equal to the feedback variable determined during block 136 above. *George, Col. 20, Line 60 to Col. 21, Line 2.*

Furthermore, in its Office Action dated June 9, 2005, the Office admits that "George does not teach a method in which one or more parity coefficients are received that are to be used to calculate the one or more parity segments..." (page 8).

From the discussion above, it is clear that George does not disclose or suggest receiving one or more parity coefficients that are to be used to calculate the one or more parity segments.

In making out a rejection of this claim, the Office admits that George does not explicitly teach writing the intermediate computation result to one or more local buffers. However, the Office finds that this would have been obvious over George as a matter of design choice. The Applicant disagrees. George does not teach the use of parity coefficients as discussed above. Therefore, George also fails to teach operating on the one or more data

segments and the one or more ***parity coefficients*** to provide an ***intermediate computation result***. As such, the intermediate computation result cannot be calculated because it depends on the parity coefficients. Therefore, it would be impossible for George to write the intermediate computation result to one or more local buffers on the ASIC.

Accordingly, for at least these reasons, this claim is allowable.

Claim 14 depends from claim 13 and is allowable as depending from an allowable base claim. This claim is also allowable for its own recited features which, in combination with those recited in claim 13, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Claim 15 recites a method of calculating parity segments comprising [emphasis added]:

- providing a parity calculation module configured to calculate one or more parity segments;
- with the parity calculation module:
  - receiving one or more data segments that are to be used to calculate one or more parity segments;
  - ***receiving one or more parity coefficients that are to be used to calculate the one or more parity segments;***
  - operating on the one or more data segments and the one or more parity coefficients to provide an intermediate computation result;
  - writing the intermediate computation result to one or more local buffers; and
  - ***within one clock cycle of an associated clock, receiving (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operating on them to provide a result that is stored in the one or more local buffers.***

For the same reasons as discussed above, this claim is allowable. George does not disclose or suggest receiving one or more parity coefficients that are to be used to calculate the one or more parity segments.

Additionally George does not disclose or suggest a method which, within one clock cycle of an associated clock, receives (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operates on them to provide a result that is stored in the one or more local buffers. The Office has already disagreed with this argument in its June 9, 2005 Office Action. In that Office Action, the Office states:

> In George's reference, after incrementing the index j, the processing of parity calculation continues again (column 12 line 56-column 13 line 4). In other words, the receiving of a variable for feedback and a previously calculated parity digital is performed again.

The excerpt cited by the Office above (column 12 line 56-column 13 line 4) is reproduced below for the convenience of the Office:

> Processing continues at block 148, during which the parity block index j is incremented by 1. Then, during block 140, the parity block index j is compared with the redundancy variable r to determine if they are equal. Assuming that j is equal to r, processing continues at block 142, during which the last parity digit to be calculated for the currently processed byte of data is determined by the equation:
>
> parity(PARBLK+j-1, i)=g(r-j) * FDBK
>
> where the variables referenced have been described above. During block 146, processing returns to FIG. 5 at block 126. A more detailed discussion regarding calculation of parity digits will be discussed with reference to the results table in FIGS. 10(A), (B) and (C).

The Applicant fails to understand how this excerpt discloses a method which, ***within one clock cycle of an associated clock***, receives (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operates on them to provide a result that is stored in the one or more local buffers.

Furthermore, there is no mention whatsoever in the excerpt cited by the Office or in George itself, of clock cycles. Accordingly, George does not disclose a method which, ***within one clock cycle of an associated*** clock, (a) the intermediate computation result from the one or more local buffers, (b) one or more additional data segments and (c) one or more additional parity coefficients, and operates on them to provide a result that is stored in the one or more local buffers.

Accordingly, for at least these reasons, this claim is allowable.

Claims 16-19 depend either directly or indirectly from claim 15 and are allowable as depending from an allowable base claim. These claims are also allowable for their own recited features which, in combination with those recited in claim 15, are neither shown nor suggested in the references of record, either singly or in combination with one another.

Conclusion

All of the claims are in condition for allowance. Accordingly, Applicant requests a Notice of Allowability be issued forthwith. If the Office's next anticipated action is to be anything other than issuance of a Notice of

5 Allowability, Applicant respectfully requests a telephone call for the purpose of scheduling an interview.

Respectfully Submitted,

10 Dated: 8/29/05 By: _____

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